Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of claims:

1-4. (Canceled).

5. (Previously presented) A method of stress testing an integrated circuit, comprising:

capturing a external bus transaction,

if a request type of the transaction matches a triggering condition, generating a data request, and

generating a harassing bus transaction based on the data request.

6. (Previously presented) The method of claim 5, wherein the external bus transaction and the harassing bus transaction are generated by the same integrated circuit.

7. (Previously presented) The method of claim 5, wherein the data request includes an address contained in the external bus transaction.

8. (Original) The method of claim 5, wherein the external bus transaction includes a first cache line address in a system memory and the data request includes a second cache line address adjacent to the first cache line address.

9. (Previously presented) The method of claim 5, wherein the external bus transaction includes an address directed to a first portion of a cache line in a system memory and the data request includes a second address directed to a second portion of the cache line.

10. (Previously presented) The method of claim 5, wherein the harassing bus transaction is generated before the external bus transaction concludes.

11-17. (Canceled).

18. (Previously presented) A stress testing method for a computer system, comprising:

counting a number of external bus cycles that occur without onset of a new transaction on the external bus,

determining if the number meets a threshold value, and

if so, generating a harassing transaction on the external bus.

19. (Original) The method of claim 18, wherein the harassing transaction includes an address from a previous bus transaction having been modified to refer to an adjacent cache line.

20. (Previously presented) An integrated circuit, comprising:

a processor core, the processor core to operate in the domain of a first clock,

a data request pipeline having an external bus interface coupled to an external bus, the external bus to operate in the domain of a second clock, where the second clock is different from the first clock, and

a validation functional unit block (FUB) having an input coupled to the external bus interface of the data request pipeline, the validation FUB to operate in the domain of the first clock, the validation FUB further comprising:

a transaction latch coupled to the external bus interface, and

a request library coupled to the transaction latch and having an output coupled to the data request pipeline, to store transaction request types according to an external bus protocol.

21. (Previously presented) The integrated circuit of claim 20, wherein the first clock is faster than the second clock.

22. (Canceled).

23. (Previously presented) The integrated circuit of claim 20, further comprising an address manipulator coupled to the transaction latch and to the request library.

24. (Previously presented) An integrated circuit, comprising:

a processor core,

a bus sequencing unit coupled to the processor core and an external bus, the bus sequencing unit comprising:

an arbiter to receive a first data request,

a cache memory to store data, and

a transaction queue coupled to the arbiter and the cache memory to process the first data request, and

a validation functional unit block (FUB) coupled to the bus sequencing unit and the external bus, the validation FUB to receive the first data request from the arbiter to generate a second data request if the first data request matches a triggering condition.

25. (Previously presented) The integrated circuit of claim 24, where an output of the validation FUB is coupled to the arbiter.

26. (Previously presented) The integrated circuit of claim 25, wherein the arbiter processes the first data request and the second data request as independent transactions.

27. (Previously presented) A computer system, comprising:

a processor core,

a bus sequencing unit coupled to the processor core and an external bus, the bus sequencing unit further comprising:

an arbiter to receive a first data request,

a cache memory to output a hit/miss signal in response to the first data request, and

a transaction queue coupled to the arbiter and the cache memory to process the first data request, and

a validation functional unit block (FUB) coupled to the bus sequencing unit and the external bus, the validation FUB to receive the hit/miss signal from the cache memory to generate a second data request if the hit/miss signal matches a triggering condition.

28. (Previously presented) The system of claim 27, wherein the triggering condition is whether requested data is present in the cache memory.

29. (Currently Amended) A diagnostic method for an integrated circuit, comprising:

detecting an onset of a first transaction on an external bus,

reading an address of the first transaction from the external bus, and

in response to the detected transaction, issuing a read request in a second transaction on the external bus, the read request directed to the ~~same~~ address read from ~~as the~~ said first transaction from the external bus.

30. (Previously presented) The method of claim 29, wherein an onset of the second transaction occurs before the first transaction concludes.

31. (Previously presented) The method of claim 29, further comprising issuing a plurality of read requests directed to addresses of subsequent transactions detected on the external bus.

32. (Previously presented) The method of claim 29, wherein the first and second transactions are issued by the same integrated circuit.

33-35. (Canceled).

36. (Currently amended) A method of testing an integrated circuit, comprising:

storing a request type in a register,

observing a transaction on an external bus, and

~~when~~ if the request type of the external bus transaction matches the request type stored in the register, generating a data request on the external bus.

37. (Currently amended) The method of claim 36, ~~further comprising generating~~ wherein the data request on the external bus is a harassing bus transaction ~~based on the data request~~.

38. (Previously presented) The system of claim 27, where an output of the validation FUB is coupled to the arbiter.

39. (Previously presented) The system of claim 38, wherein the arbiter is to process the first data request and the second data request as independent transactions.

40. (Currently amended) A system comprising:

a data bus;

means for latching transaction data observed on the data bus, the transaction data to include a first data request to a first data address;

means for determining whether a type of the first data request latched by said means for latching satisfies a trigger condition;

means for forming a second data request based on the first data address if said means for determining determines that the trigger condition is satisfied; and

means for posting the second data request to the data bus as a harassing transaction.

41. (Previously presented) The system of claim 40, wherein said means for forming the second data request is to form the second data request by appending the first data address onto a request pattern.

42. (Previously presented) The system of claim 40, further comprising:

means for incrementing or decrementing the first data address,

wherein said means for forming the second data request is to form the second data request by appending the incremented or decremented first data address onto a request pattern.